

Information Disclosure Statement
USSN 09/768,904
September 24, 2003
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Form PTO-1449 (Modified)	ATTY DOCKET NO. B-3964 618029-8	U.S. SERIAL NO. 09/768,904
LIST OF PATENTS AND PUBLICATIONS STATEMENT	APPLICANT(S) Lap-Wai Chow, et al.	
	FILING DATE January 24, 2001	GROUP 2815

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	ISSUE DATE	NAME	CLASS	SUBCLASS	FILING DATE or 102(e) DATE IF APPROPRIATE
/JN/	5,895,241	4/1999	Lu et al.	438	275	

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	PUBLICATION DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES/NO
/JN/	0 186 855 A2	7/1986	EP			
↓	1 193 758 A1	4/2002	EP			
↓	1 202 353 A1	5/2002	EP			
↓	61-147551	7/1986	JP			
↓	98/57373	12/1998	WO			

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

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EXAMINER	DATE CONSIDERED
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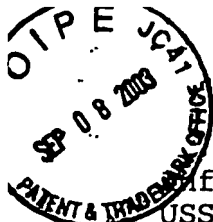
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/JN/	4,322,736	3/1982	Sasaki et al.	257	369	
	5,177,589	1/1993	Kobayashi et al.	257	773	
	5,225,699	7/1993	Nakamura	257	306	
	5,317,197	5/1994	Roberts	257	401	
	5,345,105	9/1994	Sun et al.	257	659	
	5,404,040	4/1995	Hshieh et al.	257	341	
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	5,677,557	10/1997	Wuu et al.	257	382	
	5,821,590	10/1998	Lee et al.	257	377	
	5,854,510	12/1998	Sur, Jr., et al.	257	529	
	5,888,887	3/1999	Li et al.	438	525	
	5,930,667	7/1999	Oda	438	622	
	5,998,257	12/1999	Lane et al.	438	253	
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/JN/	0 186 855 A2	7/1986	EP			
↓	0 920 057 A2	6/1999	EP			
↓	10-256398	9/1998	JP			abstract
↓	61-147551	7/1986	JP			abstract
↓	98/57373	12/1998	WO			abstract

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

/JN/	Blythe, et al., "Layout Reconstruction of Complex Silicon Chips," <i>IEEE Journal of Solid-State Circuits</i> , pp. 138-145 (February 1993).
/JN/	Ng, K.K., <i>Complete Guide to Semiconductor Devices</i> , McGraw-Hill, Inc., pp 164-165 (1995).
/JN/	IBM_TDB, "Double Polysilicon Dynamic Memory Cell with Polysilicon Bit Line," pp 3828-3831 (February 1979).
/JN/	IBM_TDB, "Static Ram Double Polysilicon Process," pp 3683-3686 (January 1981).

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